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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/655,937	09/06/2000	Jong Sang Baek	8733.289.00	8624

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EXAMINER
NELSON, ALECIA DIANE

ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 10/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/655,937	BAEK ET AL.	
	Examiner	Art Unit	
	Alecia D Nelson	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. ***Claims 1, 2, 4, 6, 8, 9, 11, and 20*** are rejected under 35 U.S.C. 102(e) as being anticipated by Shin (U.S. Patent No. 6,323,836).

With reference to **claims 1, 8, and 20**, Shin teaches a liquid crystal display device (100), comprising a line memory (230) for dividing a data for at least one line inputted from the exterior thereof into a plurality of groups to store the divided data therein and for outputting the data at a desired unit from each of the groups; a driving circuit (270) including n driver integrated circuits (240, 250) that are connected to the line memory (230) and the liquid crystal display panel (100) to drive the liquid crystal display panel in response to the data outputted from the line memory (230); and a timing controller (220), being connected to the line memory (230) and the driving circuit (270), for receiving a data clock inputted from the exterior thereof to output the data from the plurality of groups of the line memory (230) to the driving circuit (270) every

period of the data clock in response to a time corresponding to the number of said groups (see column 5, line 18-column 6, line 18). With further reference to **claims 8 and 20**, Shin teaches, with reference to the summary of the invention, generating a first data clock by frequency-dividing the data clock at a frequency-division ratio corresponding to the number of divided groups (see column 3, lines 53-62).

With reference to **claims 2 and 9**, Shin teaches, with reference to FIG. 4, a first group (A) and a second group (B), wherein the data driver ICs are divided also into the two groups (A, B) and the video data are sent to and latched at the two groups (see col. 2, lines 43-54).

With reference to claim with reference to **claims 4, 6, and 11**, Shin teaches, with reference to FIG 5, that the data driver ICs are divided into two groups. One group, an odd data driver IC group (32), is the driver for ICs connected with the odd numbered data lines. The other group, an even data driver IC group (33), is for the driver ICs connected to the even numbered data lines (see column 2, lines 56-64).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 5, 7, 10, 12-19, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. (U.S. Patent No. 6,362,804) in view of Park (U.S. Patent No. 6,040828).

With reference to claims 3, 5, 7, 10, and 12 Park et al. teaches a liquid crystal display apparatus and method for displaying a picture different in aspect ratio than the liquid crystal panel (see abstract). Park et al. teaches a line memory (not shown) which writes the digital data to the data converter (30). The input picture data IDA is a digitization of an analog image signal performed by an analog to digital converter, and is supplied to the data converter (30) via a memory. The picture data is written to the data converter (30) by the memory at twice the sampling clock frequency of an analog to digital converter (see column 4, lines 49-55). There is taught a driving circuit (DD1-10, GD1, GD2) connected to the converter (30) and a liquid crystal panel (10) (see column 3, lines 6-11), and a timing controller (20) connected to the data converter (30) and the driving circuits for receiving a data clock (CLK) from an exterior thereof to output the data from the data converter to driver circuits.

Park et al. fails to specifically teach that the timing controller generates an inverted data clock having a phase contrary to the input data clock.

Park teaches a liquid crystal display device wherein the driving circuit includes a clock generator processing a first clock signal to output a second clock signal, the clock speed of the second clock signal being half of that of the first clock signal, a memory for storing a first video data and a second video data in accordance with the first clock signal, and a data controller for simultaneously outputting the first video data and the

second video data stored in the memory in accordance with the second clock signal (see abstract). There is also taught that a gate shift clock (GSC) signal is input of the shift registers (SR-SRn) and the logic gates (AND1-AND2n) are AND gates, which are alternatively applied with the GSC signal and with the inverted gate, shift clock (GSC') signal. When the GSC signal and its inverted signal GSC' are synchronously applied, the gate (G1) is driven during the positive trigger of the gate shift clock signal GSC, and the gate (G2) is driven during the positive trigger of the inverted signal GSC' of the GSC signal. Consequently, two corresponding gate pulses of the gate driver IC are sequentially enabled in a horizontally synchronous interval (see column 5, lines 1-34).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to include an two clock signals, one having a phase contrary to the input data clock, as taught by Park, in a system similar to that which is taught by Park et al., in order to provide a liquid crystal device in which the video data of two data lines can be driven thereby improving the display quality of the liquid crystal display.

With reference to **claims 13-19** Park et al. teaches a liquid crystal display apparatus and method for displaying a picture different in aspect ratio than the liquid crystal panel (see abstract). Park et al. teaches a line memory (not shown) which writes the digital data to the data converter (30). The input picture data IDA is a digitization of an analog image signal performed by an analog to digital converter, and is supplied to the data converter (30) via a memory. The picture data is written to the data converter (30) by the memory at twice the sampling clock frequency of an analog to digital

converter (see column 4, lines 49-55). There is taught a driving circuit (DD1-10, GD1, GD2) connected to the converter (30) and a liquid crystal panel (10) (see column 3, lines 6-11), and a timing controller (20) connected to the data converter (30) and the driving circuits for receiving a data clock (CLK) from an exterior thereof to output the data from the data converter to driver circuits.

Park et al. fails to specifically teach outputting two pixel data in each of the groups to the driving circuit during each period of the first data clock.

With further reference to **claims 15, 17, and 19**, Park teaches a liquid crystal display device wherein the driving circuit includes a clock generator processing a first clock signal to output a second clock signal, the clock speed of the second clock signal being half of that of the first clock signal, a memory for storing a first video data and a second video data in accordance with the first clock signal, and a data controller for simultaneously outputting the first video data and the second video data stored in the memory in accordance with the second clock signal (see abstract). There is also taught that a gate shift clock (GSC) signal is input of the shift registers (SR-SRn) and the logic gates (AND1-AND2n) are AND gates, which are alternatively applied with the GSC signal and with the inverted gate shift clock (GSC') signal. When the GSC signal and its inverted signal GSC' are synchronously applied, the gate (G1) is driven during the positive trigger of the gate shift clock signal GSC, and the gate (G2) is driven during the positive trigger of the inverted signal GSC' of the GSC signal. Consequently, two corresponding gate pulses of the gate driver IC are sequentially enabled in a horizontally synchronous interval (see column 5, lines 1-34).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to include an two clock signals, one having a phase contrary to the input data clock, as taught by Park, in a system similar to that which is taught by Park et al., in order to provide a liquid crystal device in which the video data of two data lines can be driven thereby improving the display quality of the liquid crystal display

Response to Arguments

Applicant's arguments filed 7/29/02 with respect to **claims 1, 2, 4, 6, 8, 9, 11, and 20** have been fully considered but they are not persuasive. The applicant argues that Shin fails to teach a timing controller as recited in **claims 1, 8, and 20**. Shin clearly teaches in Fig. 8, data from the plurality of groups is outputted ever period of the data clock CK2, rather than ever other period as argued by the applicant. The timing controller receives a clock signal CK2 from the exterior thereof from the clock generator (200). The clock generator (200) having an input terminal for receiving a first clock signal CK1 and an output terminal for outputting a second clock signal CK2 (see column 5, lines 28-32). Hence data is output from the plurality of groups of the line memory (230) to the driving circuit every period of the data clock signal CK2 (see column 5, line 65-column 6, line 2).

Applicant's arguments with respect to **claims 3, 5, 7, 10, 12-19, and 21** have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D Nelson whose telephone number is (703)305-0143. The examiner can normally be reached on Monday-Friday 9:30-7:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras can be reached on (703)305-9720. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9314 for regular communications and (703)872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-9700.

adn/ADN
October 20, 2002